Proposed Final Pinout for FE Chips

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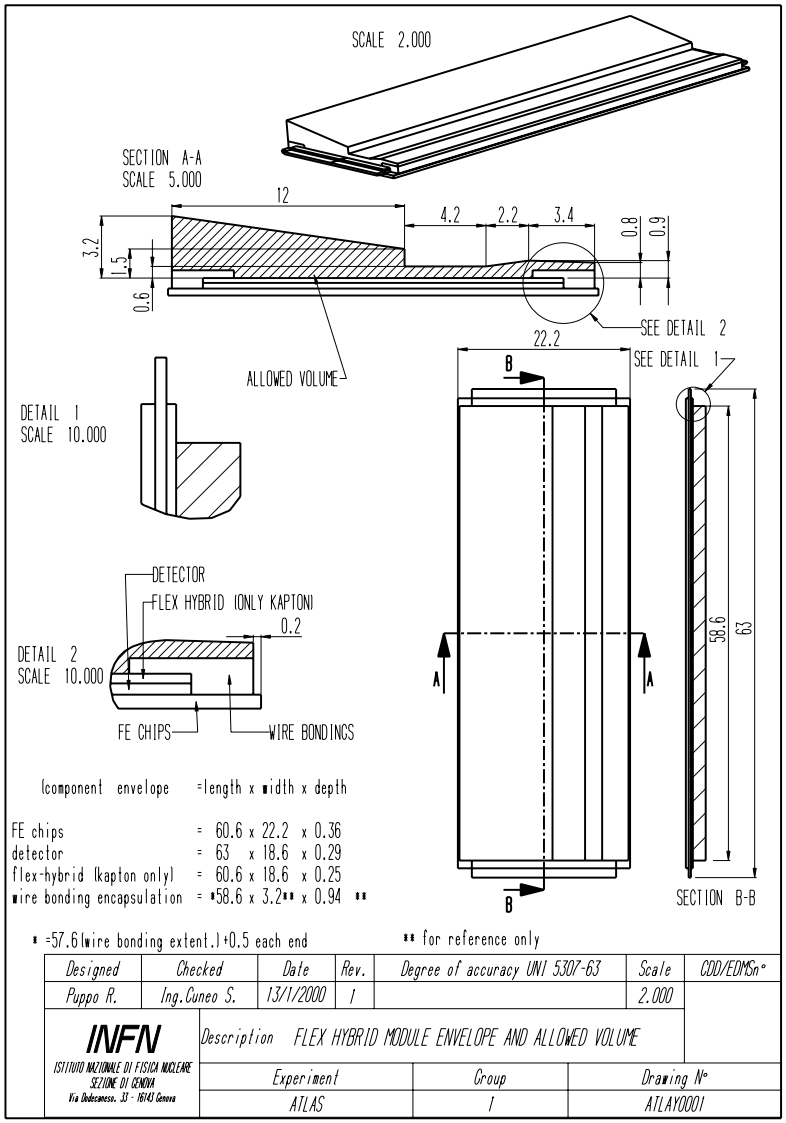
Geometry and Pinout issues:

- Need to match production pinout and geometry to proposed module envelope.

Propose final pinout, satisfying these constraints

Overview of Module Envelope

Summarize constraints on module envelope:



Constraints on FE die size:

- Present prototypes use: 7.2x(8.0+2.8)mm design size with 0.1mm dicing zone all around: 7.4x11.0mm as-cut die size.
- Production size agreed to be same: Provides total chip envelope in z of 8*7.4 + 7*0.2 = 60.6mm

Constraints on FE bonding region:

- End chips have a constraint on the region which may be wire-bonded, in order to provide good Z overlap. Bonds must fit in central 57.6mm of module, meaning central 4.4mm out of the 7.4mm as-cut die width.
- If we retain the present 150μ bond-pad spacing, that corresponds to 30 bonding pads (4.35mm + pad size).

Proposed Final FE Chip Pinout (30 bonded pads):

- Total of 10 power pins, positioned at 1/4 and 3/4 points in die (mirror or not ?) :

  p11, p38 VDDA
  p12, p37 VCCA
  p13, p36 AGnd
  p14, p35 DGnd
  p15, p34 DVdd

- Total of 9 Command and Address pins:

  p16 CCK
  p17 DI
  p18 LD
  p19, p20 STRn, STRp
  p21 - p24 GA0 - GA3

- Total of 1 analog pin (may become optional if new chopper works very well):

  p25 VCal

- Total of 6 control pins:

  p26, p27 SYNCn, SYNCp
  p28, p29 XCKn, XCKp
  p30, p31 LV1n, LV1p

- Total of 2 output pins

  p32, p33 DOn, DOp

- Total of 2 detector pins:

  p10 DGuard
  p39 DGrid

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To reach this, have removed 18 pads from present pinout:

- RSTb and Shield, and Analog pins (I1-I8, and VCCD/VTH)
- All monitoring pins (MonHit, MonSel, MonRef, MonAmp)
- Propose to retain most on the die, in locations compatible with present floorplans:
- Total of 1 control pin:

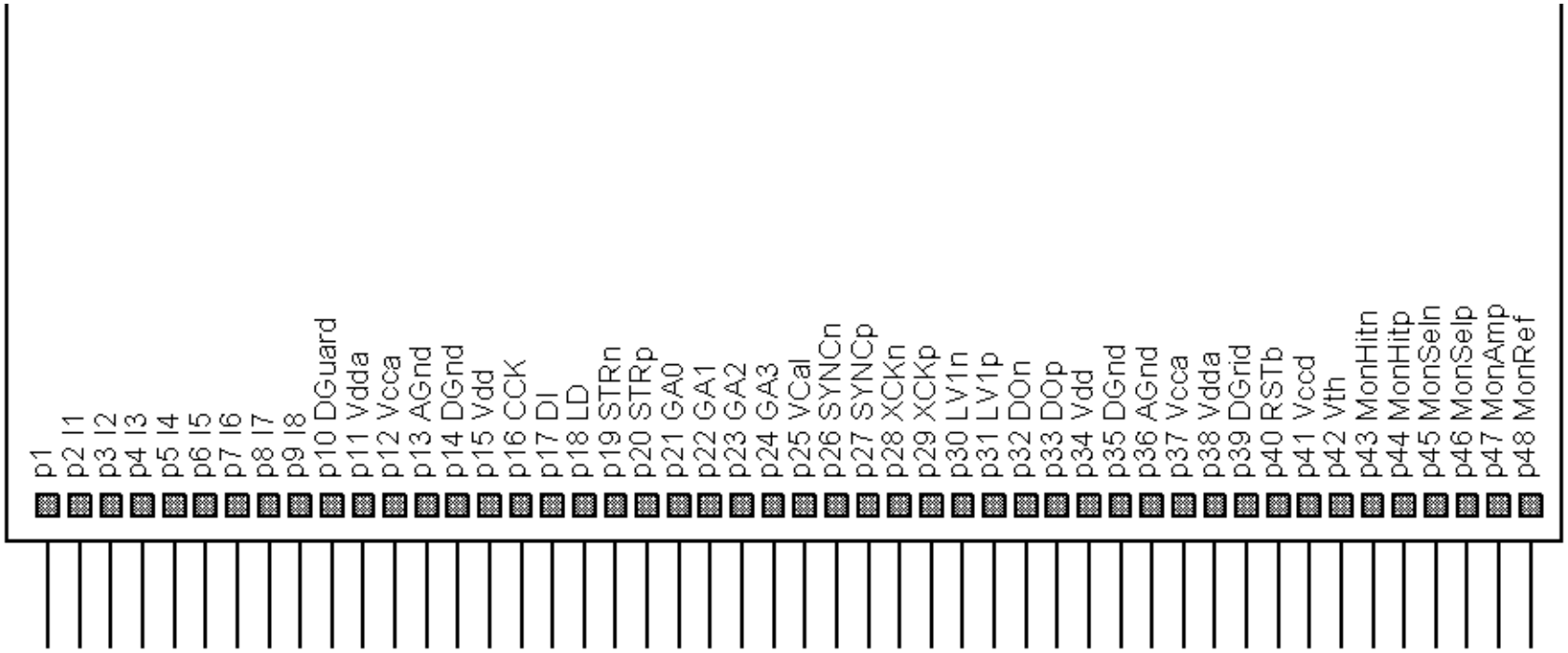
  p40 RSTb
- Total of 8 current monitor pins:

  p2 I1
  p3 I2
  p4 I3
  p5 I4
  p6 I5
  p7 I6
  p8 I7
  p9 I8
- Total of 2 voltage monitor pins and 6 special monitoring pins:

  p41 VCCD
  p42 VTH
  p43, p44 MonHitn, MonHitp
  p45, p46 MonSeln, MonSelp
  p47 MonAmp
  p48 MonRef

Proposed Pad Geometry:

- Retain present 100µ x 100µ pad size, with 150µ pitch
- Continue to locate pads close to the lower die edge, as for demonstrator chips.
- The present demonstrator geometry has 48 pads, with centers along a line 175µ above the bottom (referenced to the as-cut die size of 7.4x11.0mm). The first pad center is also 175µ from the vertical edge referenced to the as-cut die size.
- Propose that this pad placement would be retained, and only the central 30 pads would be used for production bonding:



Overall Chip Geometry: